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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ROSS, JOHN M	

ART UNIT	PAPER NUMBER
2188	9

DATE MAILED: 04/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/836,593	PENNEY ET AL.	
	Examiner	Art Unit	
	John M Ross	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings filed on 16 April 2001 have been approved by the Examiner.

Specification

2. The disclosure is objected to because of the following informalities:

The word "burst" has been misspelled as "bust" in numerous instances throughout the specification. For example, lines 14 and 24 on page 6, line 1 on page 9, and line 10 on page 10, all in the original specification. All such misspellings must be corrected.

The specification makes reference to element "48a,b" in line 2 on page 6 of the Supplemental Preliminary Amendment, however there is no corresponding element in Fig. 1 of the drawings. The element reference should be "48".

Lines 12-14 on page 4 of the Supplemental Preliminary Amendment state, "In all of the above cases, the sequence of column addresses can be generated by an incrementing a burst counter that generates only the NLSB..." However, a decrementing sequence is shown on page 2 of the Supplemental Preliminary Amendment.

Lines 19-23 on page 4 of the Supplemental Preliminary Amendment should have a "0" rather than a "1" in the first column of the column address.

Appropriate correction of the above noted deficiencies is required.

Claim Objections

3. Claims 15-17 are objected to because of the following informalities:

The second instance of the word "receiving" in line 18 of claim 15 is redundant and should be deleted.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-3, 6-11, 15-21, 25-28 and 30-33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject

matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification discloses a single burst counter for generating a column address in both serial and interleaved modes of operation in a memory device that utilizes a 2-bit prefetch (Page 6, lines 1-5 in the original specification). Applicant admits in the "BACKGROUND OF THE INVENTION" that similar memory devices are known in the art that utilize two separate counters, one for each mode of operation (Page 1, line 1 to page 2, line 7 in the original specification; Suppl. Pre Amdt., pages 1-2 and page 5, lines 9-13).

Applicant further contemplates two problems: divergent even/odd column address pairs in serial mode (Suppl. Pre Amdt., page 4, lines 12-23; page 4, line 25 to page 5, line 5 in the original specification), and non-incrementing column addresses in interleaved mode (Page 5, lines 6-15 in the original specification; Suppl. Pre Amdt., page 5, lines 3-6).

Applicant discloses a solution to the above problems comprising a single burst counter that counts up or down as a function of the burst mode, least significant column address bit (LSB) and next to least significant column address bit (NLSB) (Page 9, lines 1-12 in the original specification). Applicant asserts that "The operation of the burst counter 42 is based on the realization that the correct sequence of column addresses can be generated in the 2-bit prefetch serial mode by decrementing the column address counter whenever the LSB of the externally applied starting column address SCA<0> is a "1" " (Page 9, lines 5-8 in the original specification).

However, as may be seen in lines 7-19 on page 6 of the Supplemental Preliminary Amendment, the sequence generated is not correct. Although the problem of the divergent column address pairs has been solved, a side effect is the introduction of a new problem in that the column address does not follow a correct serial sequence. Specifically, the sequence becomes 5-4-3-2-1-0-7-6 rather than the correct serial sequence of 5-6-7-0-1-2-3-4. It is further noted that when accessing any odd starting column address in serial mode, an incorrect column address sequence will result, whereas when accessing any even starting column address in serial mode, a correct sequence will result.

Claims 1-3, 6-11, 15-21, 25-28 and 30-32 recite the features of the invention as described above that produce incorrect serial counting sequences for odd starting column addresses. Consequently, one skilled in the art clearly would not know how to use the invention embodied by these claims.

All dependent claims are rejected under the same rationale as the claims they depend from.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-3, 8-11, 18-21, 28, and 30-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The terms "serial mode" and "serial operating mode" in claims 1-3, 8-11, 18-21, 28 and 30-32 are used by the claims to mean a mode where a burst column address may increment and decrement, while the accepted meaning in the art is a mode where a burst column address always increments. The term is indefinite because the specification does not clearly redefine the term.

All dependent claims are rejected under the same rationale as the claims they depend from.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 4-5, 12-14 and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Schöniger (US 6,310,824).

As in claim 4, Schöniger discloses a burst counter for use with a 2-bit prefetch memory device having an odd memory array designated by an odd column address and an even memory array designated by an even address, the memory device capable of being operated in an interleave mode (Fig. 1; column 2, line 23 to column 3, line 40), where the burst counter comprises:

a pre-settable column address counter having a starting count input receiving all but the least significant bit of a starting column address from which the counter increments or decrements, where the counter further includes a counter control input terminal receiving a counter control signal having a first value causing the counter to increment and a second value causing the counter to decrement (Fig. 1; column 3, line 41 to column 4, line 12), where it is readily apparent that the counter operates synchronous to a clock signal (Column 2, lines 23-33); and

a counter control circuit receiving the next to least significant bit (NLSB) of the starting column address, where the counter control circuit operates to generate the second value of the counter control signal responsive to a value of "1" for the NLSB, and to generate the first value of the counter control signal responsive to a value of "0" for the NLSB (Fig. 1; column 3, lines 49-53; column 4, lines 7-12).

As in claim 5, Schöniger discloses that the counter control circuit comprises a logic circuit (Fig. 1, "AND1"; column 3, lines 49-53).

As in claim 12, Schöniger discloses a dynamic random access memory (DRAM) operable in an interleave mode (Column 2, lines 23-36) comprising:

an even array and an odd array of memory cells arranged in rows and column (Fig. 1, "MA"; column 2, lines 41-55; column 3, lines 27-29);

a row decoder coupled to receive row addresses and being operable to activate a row of memory cells corresponding to the row address (Fig. 1, "RDEC"; column 2, lines 45-47); and

a column address decoder coupled to receive a column address and to select a column of memory cells in each array corresponding to the column address (Fig. 1, "CDEC1", "CDEC2"; column 2, lines 47-52);

where it is inherent in Schöniger that a data path couples the memory arrays to a data bus, and that a command decoder receives memory commands from a command bus and generates control signals corresponding to the memory commands, because the embodiment of Schöniger is described as a synchronous dynamic random access memory (SDRAM) (Column 2, lines 23-27), which is a device known in the art to couple the memory array to a data bus in order to provide data externally to the device, and which is also well known to receive encoded commands that must be decoded in order for the device to respond according to the command.

Further regarding claim 12, the rationale derived from Schöniger in the rejection of claim 4 is incorporated herein for the teaching of a pre-settable counter and a counter control circuit.

As in claim 13, Schöniger discloses that the DRAM is an SDRAM (Column 2, lines 23-27).

Claim 14 is rejected using the same rationale as for the rejection of claim 5 above.

Method claim 29 is rejected using the same rationale as for the rejection of claim 4 above.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schöniger (US 6,310,824).

As to claim 22, the rationale derived from Schöniger in the rejection of claim 12 above, is incorporated herein for the teachings related to a dynamic random access memory (DRAM) operable in an interleave mode.

Regarding claim 22, although Schöniger does not explicitly teach that the DRAM is included in a computer system further comprising computer circuitry operable to perform computing functions, coupled to at least one input and one output device, and at least one data storage device, Examiner takes Official Notice that computer systems so comprised are well known in the art as useful for performing a myriad of general purpose computing tasks such as word-processing, and that such systems are further well known to comprise DRAM devices as a means of main storage for data. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to include the DRAM of Schöniger, in a computer system as described, in order to provide main storage for data and to allow the performance of general purpose computing tasks such as word-processing.

Claim 23 is rejected using the same rationale as for the rejection of claim 13 above.

Claim 24 is rejected using the same rationale as for the rejection of claim 5 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M Ross whose telephone number is (703) 305-0706. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMR

Gary J Portka

GARY PORTKA
PRIMARY EXAMINER